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EXAMINER	
KROFCHECK, MICHAEL C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,513	NANKI ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/764,513 filed on 1/27/2004.

2. Claims 1-10 have been submitted and examined.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

6. The abstract of the disclosure is objected to because of the phrase, "An information processing apparatus ***is disclosed***..." Correction is required. See MPEP § 608.01(b).

7. The disclosure is objected to because of the following informalities:

a. Page 1, line 21, "Linus," should be, "Linux".

Appropriate correction is required.

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

9. Claim 9 is objected to because of the following informalities:

b. The abbreviation 'DMA' should also what it represents at its first occurrence, ex. direct memory access (DMA).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the secure information unit of one of general purpose registers for storing a result of the arithmetic operation is set to a state of invalid security in when the value of the secure information unit of at least one of the two general purpose registers the arithmetic operation is performed between is in the state requiring security, but does not reasonably provide enablement for the secure information unit of one of the general purpose registers for storing the result of the arithmetic operation is set to the state of invalid security in the case where the value of the secure information unit of at least one of the general purpose registers is in the state requiring security. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to *make and use* the invention commensurate in scope with these claims.

As claimed, the GPR storing a result of an arithmetic operation is set to invalid when the state of any GPR secure, regardless if the secure GPR is involved in the arithmetic operation. From figure 6 of the specification, the result GPR is only set invalid when one of the two GPRs involved in the arithmetic operation is in a secure state.

12. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the status register further having the function of keeping the value of each flag unchanged in the case where at least one of the general purpose registers used in an arithmetic operation has the value of the secure information unit in the state requiring security at the time of the arithmetic operation

executed between at least two of the general purpose registers, but does not reasonably provide enablement for the status register further having the function of keeping the value of each flag unchanged in the case where at least one of the general purpose registers has the value of the secure information unit in the state requiring security at the time of the arithmetic operation executed between at least two of the general purpose registers. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to *make and use* the invention commensurate in scope with these claims.

This is similar to the above rejection for claim three. In this case, figure 8 of the specification shows the enabling disclosure.

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammar and idiomatic errors.

16. Take claims 1 and 2 for example. Claim 1 recites the limitations "the arithmetic operation", "the function of receiving", "the data", "the state not requiring security", "the case where the data is transferred", "the data unit", "the function of determining whether..." "the value", "the state requiring security", "the data transfer", "the function of

determining which user", "the address information" in the claim. There is insufficient antecedent basis for these limitations in the claim.

17. Claim 2 recites the limitations "the instruction code input", "the function of notifying", "the user program", "the secure program", "the function of storing", "the user", "the developer", "the contents of the secure program", and "the case where the instruction..." in the claim. There is insufficient antecedent basis for this limitation in the claim.

18. There are numerous other antecedent basis problems and grammar errors throughout the remaining claims, which are too many to mention each one specifically. The applicant is required to review the remaining claims and correct the errors in response to this correspondence.

19. Regarding claims 1 and 3, the phrase "a secure information unit added to the general purpose register" renders the claims indefinite because it is unclear what the metes and bounds of the limitation are. Is the applicant claiming that the secure information unit is stored in the general purpose register? Or that the secure information unit is functionally connected to the general purpose register?

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

21. Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by Abraham et al., US patent 5237616.

22. With respect to claim 1 Abraham teaches of an information processing apparatus for accessing memory spaces including a user memory space and a secure memory space (fig. 1; item 105, 109), comprising: a general purpose register used for the arithmetic operation of a CPU and having the function of receiving, delivering and storing the data (fig. 1; column 2, lines 45-48; the Intel 80C186 processor inherently contains general purpose registers used for arithmetic operation and I/O operation. Intel's "80C186EA/80C188EA Microprocessor User's Manual" provides support for this in sections 2.1, 2.1.3 on pages 2-1, 2-4 to 2-5);

a secure information unit added to the general purpose register and adapted to be set to the state not requiring security in the case where the data is transferred from the user memory space to the data unit of the general purpose register, and adapted to be set to the state requiring security in the case where the data is transferred from the secure memory space to the data unit of the general purpose register (fig. 2, column 3, lines 35-50);

a data control unit having the function of determining whether the value of the secure information unit is in the state requiring security or the state not requiring security when the data of the general purpose register is written in the user memory space, thereby determining whether the data transfer to the user memory space is prohibited or not (fig. 1; item 107, column 2, lines 57-67); and

an address control unit having the function of determining which of the user memory space and the secure memory space is indicated by the address information, and selecting the value of the secure information unit (fig. 1; item 210, column 3, lines 10-12).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

25. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

26. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham and Banno et al., US patent 5680581.

With respect to claim 2, Abraham teaches of an instruction buffer used by the CPU to fetch an instruction and having the function of storing therein the instruction code input from the data control unit (the 80C186 contains an instruction queue which holds the instructions until used by the CPU; "80C186EA/80C188EA Microprocessor User's Manual" provides support for this in sections 2.1.1, pages 2-2 to 2-3);

a user program arranged in the user memory space and adapted to be generated mainly by the user; and a secure program arranged in the secure memory space and adapted to be generated mainly by the developer, the contents of the secure program being not disclosed to the user (column 1, lines 54-63);

wherein the data control unit executes the data transfer from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction in such a manner that the data transfer to the user memory space is prohibited in the case where the value of the secure information unit is in the state requiring security (column 2, lines 50-67).

Abraham fails to explicitly teach of an instruction fetch address control unit having the function of determining which of the user memory space and the secure memory space is indicated by the address information.

However, Banno teaches of an instruction fetch address control unit having the function of determining which of the user memory space and the secure memory space is indicated by the address information when storing the instruction code input from the data control unit (column 3, lines 43-51), and

the function of notifying the data control unit which of the user program and the secure program is under execution (column 2, lines 5-9);

wherein the data control unit executes the data transfer from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction in such a manner that the data transfer to the user memory space is prohibited in the case where the instruction fetch address control unit determines that the instruction is fetched from the user memory space and the value of the secure information unit is in the state requiring security (column 3, lines 51-56, column 2, lines 5-9).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham and Banno at the time of the invention to prohibit reading out from the internal memory to an external memory in Abraham as taught in Banno. Their motivation would have been to prevent a third party from gaining knowledge of the internal program (column 1, lines 20-24).

27. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, US patent 6101586 and Koizumi, US patent 5414864.

28. With respect to claim 6, Abraham teaches of an information processing apparatus for accessing memory spaces including a user memory space and a secure memory space (fig. 1; item 105, 109), comprising: a secure information generating unit

for determining which of the user memory space and the secure memory space is indicated by address information (column 2, lines 57-67, as data is restricted from accessing a memory in either circumstance, it is abundantly clear to one of ordinary skill in the art that there is something that determines which memory the access is directed to through its address), and

delivering the data with secure information into a general purpose register with secure information having the function of receiving and holding the data with secure information (fig. 1; column 2, lines 45-48; the Intel 80C186 processor inherently contains general purpose registers used for arithmetic operation and I/O operation. Intel's "80C186EA/80C188EA Microprocessor User's Manual" provides support for this in sections 2.1, 2.1.3 on pages 2-1, 2-4 to 2-5);

a built-in memory space for receiving and holding the data with secure information from the general purpose register and delivering the data thus held to the general purpose register (fig. 1; item 105, 109); and

a data output control unit having the function of controlling the data transfer to an external space by the secure information (column 2, lines 57-67);

wherein the data output control unit performs the control operation to determine whether the data transfer to the external space is prohibited or not by the value of the secure information (column 2, lines 57-67; column 3, lines 10-12).

Abraham fails to explicitly teach of the built-in memory space being a RAM. However, Ishimoto teaches of the built-in memory space being a RAM (column 11, lines 46-49).

Abraham fails to explicitly teach of the value of the secure information being set in the general purpose register. However, Koizumi teaches of a status value being set in the general purpose register (column 2, lines 36-42);

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham and Ishimoto at the time of the invention to use RAM as the unprivileged memory in Abraham as taught in Ishimoto, since RAM is the most commonly available and most versatile type of memory.

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, and Koizumi at the time of the invention to indicate the privileged and unprivileged states in the GPR of Abraham as taught in Koizumi so the status is directly accessible by the processor.

29. Claim 7-8, 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi, Banno, and Garney, US patent 5386552.

With respect to claim 7, the combination of Abraham, Ishimoto, and Koizumi teach of the limitations cited above with respect to claim 6.

Abraham fails to explicitly teach of delivering an instruction with secure information into an instruction decoder with secure information having the function of determining which of the user memory space and the secure memory space is associated with the instruction under execution.

However, Banno teaches of delivering an instruction with secure information into an instruction decoder with secure information having the function of determining which

of the user memory space and the secure memory space is associated with the instruction under execution (column 3, lines 44-51);

Abraham fails to explicitly teach of an interrupt saved information unit with secure information having the function of adding, upon generation of an interrupt process, the secure information of the instruction decoder to the data saved in the stack area of the built-in RAM space.

However, Garney a built-in RAM space with secure information for receiving and holding the data with secure information from the general purpose register and delivering the data thus held to the general purpose register (column 1, lines 17-40; in the combination in an interrupt processing or context switch, the GPR from the processor of Abraham are saved in the stack of Garney);

an interrupt saved information unit with secure information having the function of adding, upon generation of an interrupt process, the secure information of the instruction decoder to the data saved in the stack area of the built-in RAM space (column 1, lines 17-40).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, and Banno at the time of the invention to identify the memory associated with the requested instruction in the combination of Abraham, Ishimoto, and Koizumi as taught in Banno. Their motivation would have been to prevent a third party from gaining knowledge of the internal program (column 1, lines 20-24).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, Banno, and Garney at the time of the invention store

the processor context upon an interrupt occurrence in the combination as taught in Garney. Their motivation would have been to enable multitasking, thus increasing the efficiency of the processor.

30. With respect to claim 8, the combination of Abraham, Ishimoto, Koizumi, Banno, Garney teach of the limitation cited above with respect to claim 7.

Garney teaches of a stack pointer for defining a part of the built-in RAM space as a stack area (column 1, lines 25-29; it is abundantly clear to one of ordinary skill in the art that a stack comprises stack pointers which define the stack); and

a saved information rewrite control unit for controlling the operation of rewriting the stack area of the built-in RAM space (column 1, lines 25-29; it is abundantly clear to one of ordinary skill in the art that since data is written to and from the stack, there must be something that controls this);

The combination of Abraham, Ishimoto, Koizumi, Banno, Garney teaches of wherein the saved information rewrite control unit prohibits the rewrite operation in the case where the instruction of the instruction decoder is associated with the user memory space and intended to rewrite the stack area of the built-in RAM space (since in the combination, writing something that does not originate within the internal memory to an internal memory is inhibited by the protection circuit of Banno, writing state information involving instruction not from the internal memory into an internal RAM stack would not be allowed).

31. With respect to claim 10, the combination of Abraham, Ishimoto, Koizumi, Banno, Garney teach of the limitation cited above with respect to claim 7.

Banno teaches of an operating unit with secure information having the function of reflecting the secure information of the instruction decoder in the arithmetic operation executed in accordance with the instruction decoded by the instruction decoder (column 1, lines 55-65, column 3, lines 44-56);

32. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Ishimoto, Koizumi and Banno.

33. With respect to claim 9, the combination of Abraham, Ishimoto, Koizumi teach of the limitations cited above with respect to claim 6.

Abraham fails to explicitly teach of a DMA with secure information having the function of holding the secure information. However, Banno teaches of a computer system including a direct memory access controller (column 1, lines 11-15).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi and Banno at the time of the invention to incorporate the DMA controller of Banno into the combination of Abraham, Ishimoto, Koizumi. Their motivation would have been to allow for data transfer to take place without the processor controlling it, thus creating more available processing time.

Allowable Subject Matter

34. Claims 3-5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st and 2nd paragraph, of themselves and their parent claims set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

35. The following is a statement of reasons for the indication of allowable subject matter:

c. With respect to claim 3, the prior art does not teach of the secure information unit of the general purpose registers storing the result of the arithmetic operation being set in an invalid security state when the value of the secure information unit of one of the general purpose registers requires security in combination with the other limitations as set forth in the claim.

d. With respect to claim 4, the prior art does not teach of a status register keeping the value of each flag unchanged when the secure information unit of one of the general purpose registers requires security in combination with the other limitations as set forth in the claim.

e. With respect to claim 5, the prior art does not teach of a debug key that when read out by the CPU through the secure IO space when the developer debugs the secure program with the user system, halts the address determining function of the instruction fetch address control unit in combination with the other limitations as set forth in the claim.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael C. Krofcheck

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